AMENDMENTS TO THE CLAIMS

1-29. (cancelled)

30. (previously presented) A phase-locked loop comprising:

a phase detector for receiving an input signal and a feedback signal, and for outputting a phase error signal based on a phase difference between the input signal the feedback signal;

a signal reshaper connected to the phase detector for reshaping the phase error signal;

a charge pump connected to the signal reshaper for receiving the reshaped or unreshaped phase error signal from the signal reshaper and for outputting a charge pump signal;

a low pass filter connected to the charge pump for receiving the charge pump signal and outputting an output signal;

a voltage-controlled oscillator connected between the low pass filter and the phase detector for receiving the output signal and for outputting a corresponding oscillation signal, wherein the feedback signal inputted into the phase detector is generated from the oscillation signal; and

a controller connected to the signal reshaper and the charge pump for controlling the signal resphaper and the charge pump;

wherein the unreshaped phase error signal causes the charge pump to output a charge pump signal that changes the frequency of the feedback signal to match the frequency of the input signal, and the reshaped phase error signal causes the charge pump to output a charge pump signal that

synchronizes the output signal with a target frequency.

31. (previously presented) The phase-locked loop of claim 30 further comprising a frequency detector connected between the voltage-controlled oscillator and the charge pump for receiving the input signal and the feedback signal and for outputting a frequency difference signal to the charge pump.

32. (previously presented) The phase-locked loop of claim 30 wherein when the frequency of the output signal is in a lower range that is lower than the target frequency, the signal reshaper reshapes the phase error signal to increase the frequency of the output signal out of the lower range; and when the frequency of the output signal is in an upper range that is above the target frequency, the signal reshaper reshapes the phase error signal to decrease the frequency of the output signal out of the upper range.

33. (previously presented) The phase-locked loop of claim 32 wherein the lower range and the upper range are frequency ranges where the unreshaped phase error signal is incapable of synchronizing the output signal with the target frequency.

34. (previously presented) The phase-locked loop of claim 30 wherein the signal reshaper is a pulse reshaper and the phase error signal comprises up pulses and down pulses.

35. (previously presented) The phase-locked loop of claim 34 wherein the pulse reshaper lengthens or shortens a period of a pulse of the phase error signal.

36. (previously presented) The phase-locked loop of claim 34 wherein the pulse reshaper increases or decreases a width of a pulse.

37. (previously presented) The phase-locked loop of claim 30 wherein the charge pump increases or decreases an amplitude of a current.

38. (previously presented) The phase-locked loop of claim 30 wherein the input signal is an eight-to-fourteen modulation (EFM) signal and the output signal is a clock signal, and the phase-locked loop is incorporated into a controller of a compact disk (CD) drive or a digital versatile disk (DVD) drive.